RCLM400 DATA SHEETS

TABLE OF CONTENTS:

RCLM400 GENERAL SPECIFICATIONS.

The basic elements of RCLM400 are a series of digital integrated circuits of the TTL type (Texas Instruments Series 74 or equivalent). Specifications for these circuits are given in Appendix A.

The logic elements of RCLM400 are mainly designed from the above mentioned integrated circuits. Special elements, for example level converters, have been designed from discrete components or integrated circuits and discrete components.

The following specifications are common to all elements of RCLM400 if nothing else is separately specified.

Power Supply Voltages.

The standard power supply voltage is

+5 V ±5 per cent.

In addition, some special circuits require

+12 V ±5 per cent and/or

-6 V ±5 per cent.

Ambient Operating Temperature Range.

0 degrees C to +70 degrees C.

Logic Output Levels.

Output from a logic element will be within the following limits:

+2.4 V ≤ logical 1 ≤ +5.25 V

0 V ≤ logical 0 ≤ +0.4 V.

Logic Input Levels.

Input to a logic element should be within the following limits:

+2.0 V ≤ logical 1 ≤ +5.5 V

0 V ≤ logical 0 ≤ +0.8 V.

Unused Inputs.

Unused inputs should not be left floating, but be connected to a 1 or 0. 1 and 0 generators are placed on each card for this purpose.

Noise Margins.

The limits of input and output logic levels as stated above give the following worst-case D.C. noise margins:

at logical 1: Minimum 0.4 V
at logical 0: Minimum 0.4 V.

The typical D.C. noise margins at 25 degrees C are:

at logical 1: typ. 2.0 V
at logical 0: typ. 1.2 V.

For further description of noise margins refer to Appendix A, page 2.

Loading.

Input loading and fan-out are specified in terms of unit loads. A unit load represents a maximum of 1.6 mA out of the input at a logical 0 voltage level and a maximum of 40 µA into the input at a logical 1 voltage level.

Switching Times.

Propagation delays are measured with +1.5 V as the reference level. The following terminology is used:

td0 is the time between a change of the input signal which causes a change from 1 to 0 of the output signal.

td1 is the time between a change of the input signal which causes a change from 0 to 1 of the output signal.

Propagation delays are specified at the following operating conditions:

Vcc = +5.0 V
Ta = 25 degrees C
Maximum fan-out
Load capacitance = 15 pF.

For specification of propagation delays at other operating conditions are referred to Appendix A, page 5059.

Mechanical.

The circuits are mounted on glass-epoxy printed circuit boards, 4.3x5.8 inches. The cards are provided with an ELCO VARICON connector plug with 41 pins, which mate with an ELCO VARILOK receptacle.

Outputs from the circuits on the card are normally connected to test points which are placed at the back edge of the cards.

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Author: Aa. Jørgensen
Edited: February 1969

RC STANDARD

FOR CIRCUIT CLASSIFICATION

A/S REGNECENTRALEN
Falkoneralle 1
Copenhagen F.

CIRCUIT ELEMENT CLASSIFICATION SYSTEM.

This classification code will be used for electronic circuits applied in equipment developed at A/S Regnecentralen.

The code consists of two letters followed by three digits.

First letter:	A. Combinatorial networks B. Sequential networks C. Timing circuits D. Digital interface circuits F. Analog circuits S. Special circuits
Second letter:	Subdivision of main group (see below).
First digit:	Series identification (1-9).
Second and third digit:	Serial number (01 - 49) circuits developed by department 51. Serial number (50 - 99) circuits developed by department 52.

MAIN GROUPS AND SUBDIVISIONS.

A. Combinatorial Networks.

AA AND elements
AB OR elements
AC NAND elements
AD NOR elements
AF AND-OR elements
AG AND-NOR elements
AH Logic inverter
AJ Decoding
AK Encoding
AL Adders
AM
AN
AP

B. Sequential Networks.

BA R-S bistables
BB J-K bistables
BC Type D bistables
BD Counters
BF Shift registers
BG Registers
BH
BJ

C. Timing Circuits.

CA Delay circuits
CB Monostables
CC Oscillators
CD
CF

D. Digital Interface Circuits.

DA Level converters
DB Cable transmitters
DC Cable receivers
DD Drivers (lamp drivers solenoid drivers, etc.)
DF Pulse shapers (schmitt-triggers, etc.)
DG Filter circuits
DH
DJ

F. Analog Circuits.

FA Linear amplifiers
FB Sense amplifiers
FC Analog switches
FD Digital to analog converters
FF Power supply supervision
FG
FH

S. Special Circuits.

SA
SB

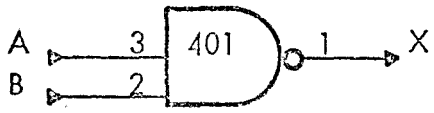
Examples:

AC401: 2-input NAND element from the RCLM400 series of digital logic modules.

AC402: 4-input NAND element from the RCLM400 series of digital logic modules.

BB401: J-K bistable from the RCLM400 series of digital logic modules.

AC401



CIRCUIT DESCRIPTION

The AC401 is a 2-input NAND element. The logical operation of the element is:

$$X = -_1(A \wedge B)$$

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

Input Loading	1 unit load (each input)
Fan-Out	10 unit loads

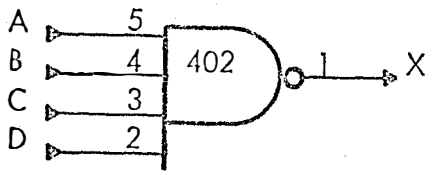
SWITCHING CHARACTERISTICS

Propagation Delay:	td1	Min. 8 ns; Typ. 18 ns; Max. 29 ns 1)
	td0	Min. 4 ns; Typ. 8 ns; Max. 15 ns 1)

NOTE

1) The indicated values for minimum propagation delay are estimated values for which the manufacturer of the circuits does not guarantee.

AC402



CIRCUIT DESCRIPTION

The AC402 is a 4-input NAND element. The logical operation of the element is:

$$X = -_1(A \wedge B \wedge C \wedge D)$$

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

Input Loading	1 unit load (each input)
Fan-Out	10 unit loads

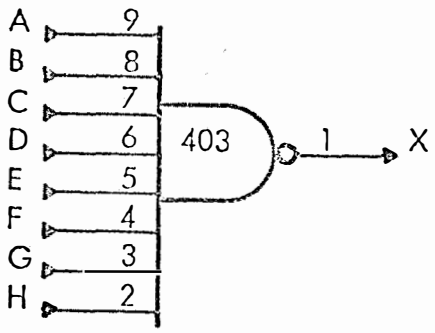
SWITCHING CHARACTERISTICS

Propagation Delay:	td1	Min. 8 ns; Typ. 18 ns; Max. 29 ns 1)
	td0	Min. 4 ns; Typ. 8 ns; Max. 15 ns 1)

NOTE

1) The indicated values for minimum propagation delay are estimated values for which the manufacturer of the circuits does not guarantee.

AC403



CIRCUIT DESCRIPTION

The AC403 is an 8-input NAND element. The logical operation of the element is:

$$X = -_1(A \wedge B \wedge C \wedge D \wedge E \wedge F \wedge G \wedge H)$$

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

Input Loading	1 unit load (each input)
Fan-Out	10 unit loads

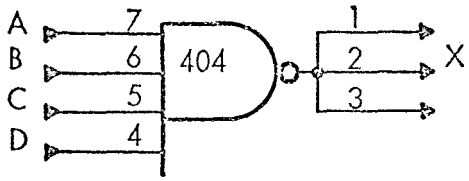
SWITCHING CHARACTERISTICS

Propagation Delay:	td1	Min. 8 ns; Typ. 18 ns; Max. 29 ns	1)
	td0	Min. 4 ns; Typ. 8 ns; Max. 15 ns	1)

NOTE

1) The indicated values for minimum propagation delay are estimated values for which the manufacturer of the circuits does not guarantee.

AC404



CIRCUIT DESCRIPTION

The AC404 is a 4-input NAND power element. The element has 3 parallel coupled output terminals, and if possible, the load should be divided equally on the 3 output terminals. The logical operation of the element is:

$$X = -,(A \wedge B \wedge C \wedge D)$$

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

Input Loading	1 unit load (each input)
Fan-Out	30 unit loads

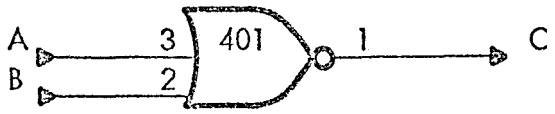
SWITCHING CHARACTERISTICS

Propagation Delay:	td1	Min. 8 ns; Typ. 18 ns; Max. 29 ns 1)
	td0	Min. 4 ns; Typ. 8 ns; Max. 15 ns 1)

NOTE

1) The indicated values for minimum propagation delay are estimated values for which the manufacturer of the circuits does not guarantee.

AD401



CIRCUIT DESCRIPTION

The AD401 is a 2-input NORelement

C = -,(A!B)

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

Input Loading	1 unit load (each input)
Fan-Out	10 unit loads

SWITCHING CHARACTERISTICS

Propagation Time	td(1)	Typ. 18 nS; Max. 29 nS
	td(0)	Typ. 8 nS; Max. 15 nS

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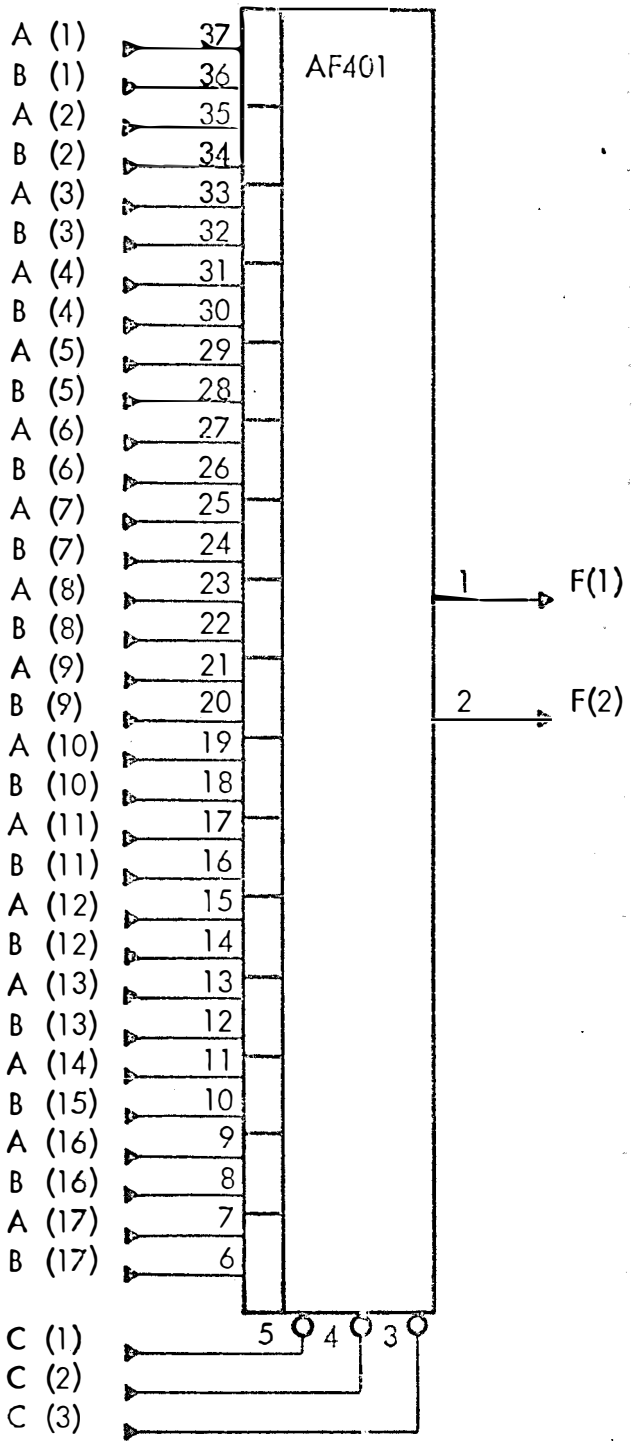
AF401



CIRCUIT DESCRIPTION

The AF401 is an AND-OR element intended for digital multiplexer applications, e.g. bus systems. The element has 16×2 inputs, A(n), B(n), and 3 expander inputs, C(1), C(2), and C(3). The number of inputs may be increased by means of AND-NOR elements connected to the expander inputs. Output is available on 2 output terminals, F(1) and F(2).

The logical operation of the AF401 is described below.

$$F(1) = F(2) = A(1) \wedge B(1) \vee A(2) \wedge B(2) \vee \ldots \vee A(16) \wedge B(16) \vee \neg C(1) \vee \neg C(2) \vee \neg C(3)$$

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

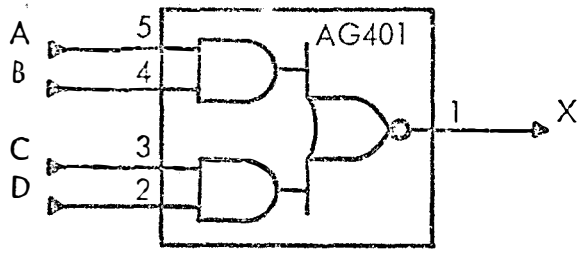
Input Loading

A(n), B(n)	1 unit load (each input)
C(1), C(2), C(3)	2 unit loads (each input)
Fan-Out, F(1), F(2)	10 unit loads (each output)

SWITCHING CHARACTERISTICS

Delay from A(n) or B(n) to F(1) or F(2), td1 = td0		Typ. 26 ns; Max. 44 ns
Delay from C(n) to F(1) or F(2)	td1	Typ. 18 ns; Max. 29 ns
	td0	Typ. 8 ns; Max. 15 ns

AG401



CIRCUIT DESCRIPTION

The AG401 is a 2×2-input AND-NOR element. The logical operation of the element is:

$$X = -_1(A \wedge B \vee C \wedge D)$$

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

Input Loading	1 unit load (each input)
Fan-Out	10 unit loads

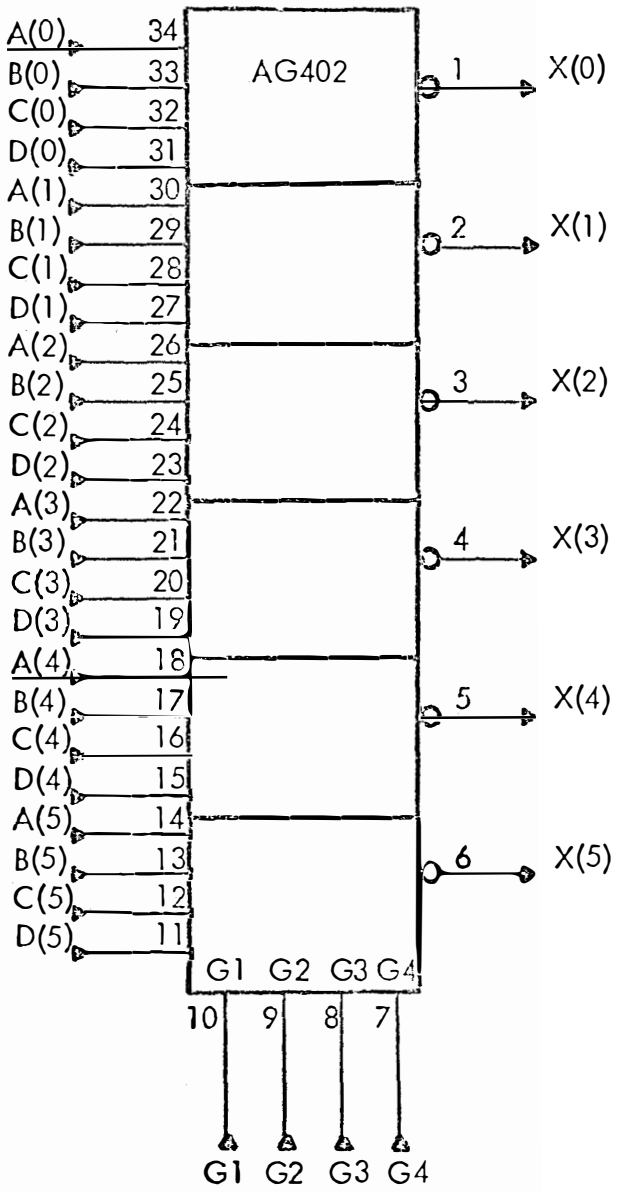
SWITCHING CHARACTERISTICS

Propagation Delay:	td1	Min. 8 ns; Typ. 18 ns; Max. 29 ns	1)
	td0	Min. 4 ns; Typ. 18 ns; Max. 15 ns	1)

NOTE

1) The indicated values for minimum propagation delay are estimated values for which the manufacturer of the circuits does not guarantee.

AG402



CIRCUIT DESCRIPTION

The AG402 is a 6-bit, 4-input digital multiplexer. The logical operation of the circuit is:

$$X(n) = -,(A(n) \wedge G1 \vee B(n) \wedge G2 \vee C(n) \wedge G3 \vee D(n) \wedge G4),$$

$$n = 0,1,2,3,4,5$$

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

Input Loading:	
A,B,C,and D inputs	1 unit load (each input)
G1,G2,G3,and G4 inputs	6 unit loads (each input)
Fan-Out	10 unit loads (each output)

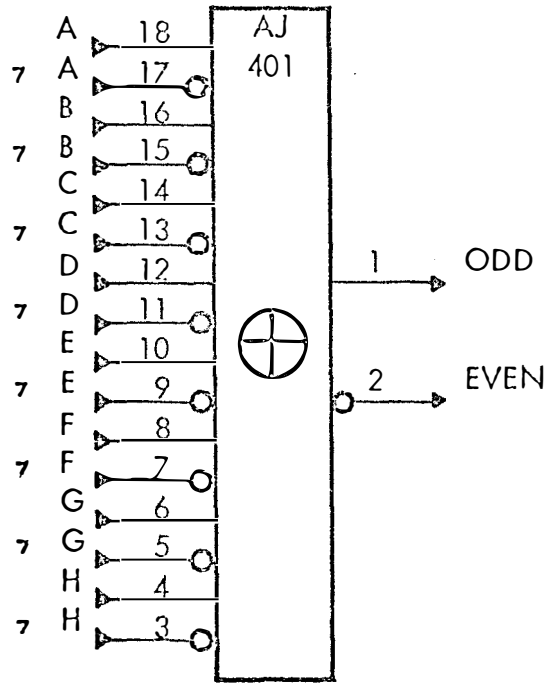
SWITCHING CHARACTERISTICS

Propagation Delay:	td1	Min. 8 ns; Typ. 18 ns; Max. 29 ns 1)
	td0	Min. 4 ns; Typ. 8 ns; Max. 15 ns 1)

NOTE

1) The indicated values for minimum propagation delay are estimated values for which the manufacturer of the circuits does not guarantee.

AJ401



CIRCUIT DESCRIPTION

The AJ401 is an 8-bit parity decoder which detects whether the input word (A,B,...,H) contains an odd or even number of 1's.

For an odd No. of 1's: ODD = 1 and EVEN = 0
For an even No. of 1's: ODD = 0 and EVEN = 1

The logical expression for the outputs is:

ODD = -,EVEN = A exor B exor C exor D exor E exor F exor G exor H

where A exor B = A $\wedge$ -,B $\vee$ -,A $\wedge$ B

SPECIFICATIONS

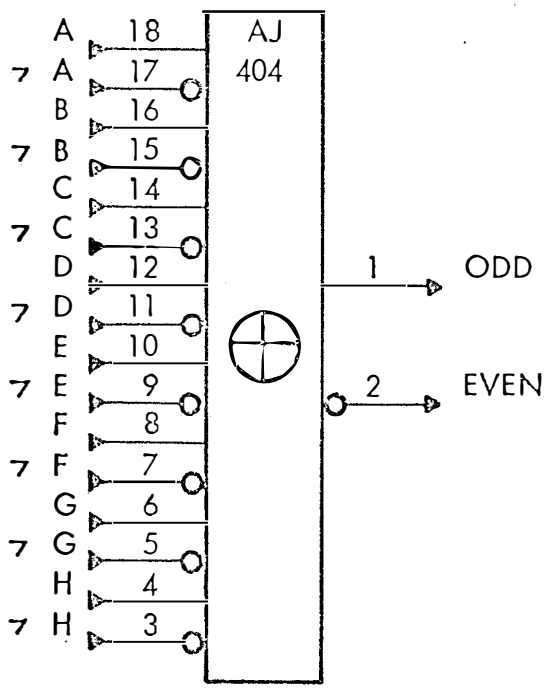
ELECTRICAL CHARACTERISTICS

Input Loading	1 unit load (each input)
Fan-Out	10 unit loads (each output)

SWITCHING CHARACTERISTICS

Delay from Input to Output:	td1	Typ. 70 ns; Max. 117 ns
	td0	Typ. 60 ns; Max. 103 ns

AJ404



CIRCUIT DESCRIPTION

The AJ404 is a high-speed 8-bit parity decoder which detects whether the input word (A,B,...,H) contains an odd or even number of 1's.

For an odd No. of 1's: ODD = 1 and EVEN = 0
For an even No. of 1's: ODD = 0 and EVEN = 1

The logical expression for the outputs is:

ODD = -,EVEN = A exor B exor C exor D exor E exor F exor G exor H

where A exor B = A $\wedge$ -,B $\vee$ -,A $\wedge$ B

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

Input Loading	1 unit load (each input)
Fan-Out	10 unit loads (each input)

SWITCHING CHARACTERISTICS

Delay from Input to Output:	td1	Typ. 53 ns; Max. 86 ns
	td0	Typ. 35 ns; Max. 62 ns

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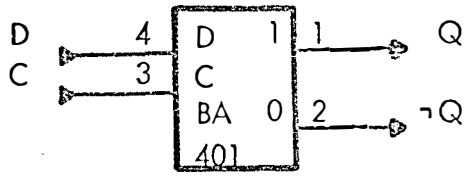
BA401



CIRCUIT DESCRIPTION

The BA401 is a bistable element of the R-S type with a data input and a control input. The operation of the element is described in the truth table below.

C	D	↓ Q
0	0	Q
0	1	Q
1	0	0
1	1	1

Q = Output before the transition from 0 to 1 of C.

↓ Q = Output after the transition from 1 to 0 of C.

When control input C is 1, the output Q will follow the data input D, (Q = D). The logic value of D is stored when C changes from 1 to 0.

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

Input Loading	
Data Input	1 unit load
Control Input	2 unit loads
Fan-Out	9 unit loads (each output)

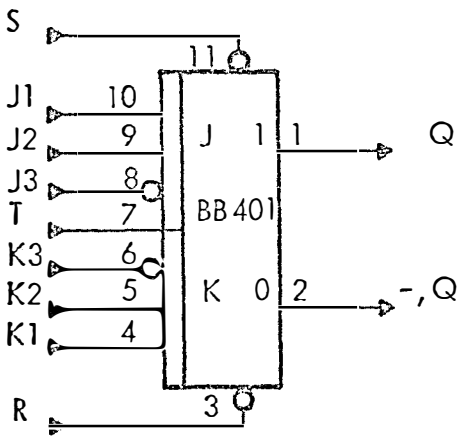
SWITCHING CHARACTERISTICS

Min. Set-Time	1)	100 ns
Delay from D to Q	td1	Typ. 26 ns; Max. 50 ns
	td0	Typ. 52 ns; Max. 100 ns
Delay from D to -,Q	td1	Typ. 44 ns; Max. 85 ns
	td0	Typ. 34 ns; Max. 70 ns

NOTE

1) To ensure correct storage of data, the control input must be 1 for a time $\geq$ Min. Set-Time. During this time the data input should remain stable.

BB401



CIRCUIT DESCRIPTION

The BB401 is an edge-triggered J-K bistable with gated J and K inputs and asynchronous reset and set inputs.

Synchronous Operation

The state of the bistable changes on the transition from 0 to 1 of the clock input T. The operation of the bistable is described in the truth table below.

J	K	↑Q
0	0	Q
0	1	0
1	0	1
1	1	-,Q

↑Q = Output after the transition from 0 to 1 of T.

J = J1 ∧ J2 ∧ -,J3

K = K1 ∧ K2 ∧ -,K3

The R and S inputs should be 1 during this mode of operation.

Asynchronous Operation

The R and S inputs are operative only when T is 0. If T is 1 when R or S changes from 1 to 0, both Q and -,Q can go to 0. When T changes to 0 the bistable will assume the state determined by the R and S inputs.

R	S	*Q
0	0	Note
0	1	0
1	0	1
1	1	Q

*Q = Next state of the bistable.

Note: Both Q and -.Q are 0, and the next state depends on the sequence in which R and S are changed.

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

Input Loading: J,K, and T	1 unit load (each input)
R and S	2 unit loads (each input)
Fan-Out	10 unit loads (each output)

SWITCHING CHARACTERISTICS

Min. Width of T	20 ns
Transition Time from 0 to 1 of T 1)	Min. 5 ns; Max. 150 ns
Min. Width of R and S	25 ns
Max. Clock Frequency	20 Mc/s
Min. Input Set-up Time 2)	20 ns
Min. Input Hold Time 3)	5 ns
Delay from T to Output	
Q or -.Q: td1	Min. 10 ns; Typ. 27 ns; Max. 50 ns
td0	Min. 10 ns; Typ. 18 ns; Max. 50 ns
Delay from R or S to Output	
Q or -.Q: td1	Max. 50 ns
td0	Max. 50 ns

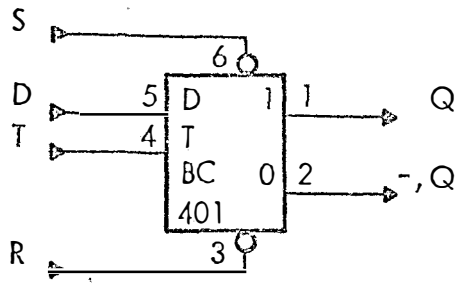
NOTES

1) Transition time from +1 volt level to +2 volts level.

2) Set-up time is the time for which the J and K inputs must be stable before the transition from 0 to 1 of T.

3) Hold time is the time for which the J and K inputs must be stable after the transition from 0 to 1 of T.

BC401



CIRCUIT DESCRIPTION

The BC401 is a D-type, edge-triggered bistable with asynchronous reset and set inputs.

Synchronous Operation

The logical value of D is stored on the transition from 0 to 1 of the clock T. Triggering occurs at a voltage level and is not directly related to the transition time of the positive edge of the clock. After the clock input threshold voltage has been passed, the D input is locked out.

D	↓Q
0	0
1	1

↓Q = Output after the transition from 0 to 1 of T.

The R and S inputs should be 1 during this mode of operation.

Asynchronous Operation

The R and S inputs are asynchronous inputs which control the state of the bistable independent of the state of the clock input T.

R	S	↓Q
0	0	Note
0	1	0
1	0	1
1	1	Q

↓ = Next state of the bistable

Note: Both Q and -,Q are 1, and the next state depends on the sequence in which R and S are changed.

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

Input Loading:	D	1 unit load
	T,S	2 unit loads (each input)
	R	3 unit loads
Fan-Out		10 unit loads (each output)

SWITCHING CHARACTERISTICS

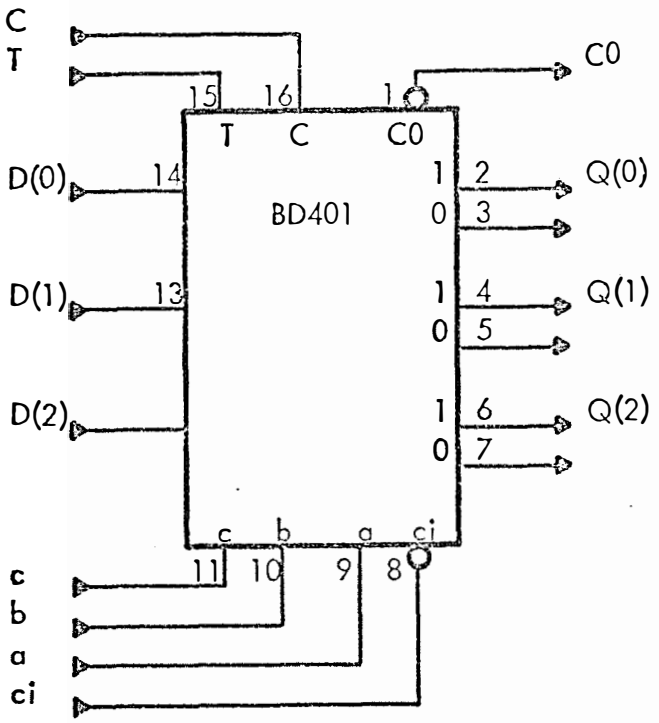
Min. Width of T		30 ns
Min. Width of R and S		30 ns
Max. Clock Frequency		15 Mc/s
Min. Input Set-up Time	1)	20 ns
Min. Input Hold Time	2)	5 ns
Delay from T to Output		
Q or ,-Q:	td1	Min. 10 ns; Typ. 20 ns; Max. 35 ns
	td0	Min. 10 ns; Typ. 28 ns; Max. 50 ns
Delay from R or S to Output		
Q or -,Q:	td1	Max. 25 ns
	td0	Max. 40 ns

NOTES

1) Set-up time is the time for which the D input must be stable before the transition from 0 to 1 of T.

2) Hold time is the time for which the D input must be stable after the transition form 0 to 1 of T.

BD401



CIRCUIT DESCRIPTION

The BD401 is a 3-bit register intended for synchronous binary counter applications. It is provided with inputs for parallel data entry.

By means of external connections the BD401 may be coupled either as a binary up-counter or down-counter. Q(2) is the least significant bit.

For operation as an up-counter, inputs a, b, and c are connected to Q(2), Q(1), and Q(0) respectively.

For operation as a down-counter, inputs a, b, and c are connected to -,Q(2), -,Q(1), and -,Q(0) respectively.

The counting sequences are shown in the truth tables below:

Up-counting						Down-counting					
Count	c0	Q(0)	Q(1)	Q(2)	ci	Count	c0	Q(0)	Q(1)	Q(2)	ci
0	1	0	0	0	0	0	0	1	1	1	0
1	1	0	0	1	0	1	1	1	1	0	0
2	1	0	1	0	0	2	1	1	0	1	0
3	1	0	1	1	0	3	1	1	0	0	0
4	1	1	0	0	0	4	1	0	1	1	0
5	1	1	0	1	0	5	1	0	1	0	0
6	1	1	1	0	0	6	1	0	0	1	0
7	0	1	1	1	0	7	1	0	0	0	0

Outputs change on the transition from 0 to 1 of the clock. Note that carry input and output are negated.

Parallel insertion of data into the register may be accomplished by means of the data inputs D(0:2) and the control input C which is common to all bits. The operation is described in the truth table below.

C	D(n)	↓ Q(n)
0	0	Q(n)
0	1	Q(n)
1	0	0
1	1	1

Q(n) = Output before the transition from 0 to 1 of C.

↓ Q(n) = Output after the transition from 1 to 0 of C.

When C is 1, output Q(n) will follow data input D(n). The logic value of D(n) is stored when C changes from 1 to 0.

Clock input should be 0 during this mode of operation.

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

Input Loading

D(0:2), c	1 unit load (each input)
T, b	3 unit loads (each input)
a	5 unit loads
C	6 unit loads
ci	7 unit loads

Fan-Out		10 unit loads (each output)

SWITCHING CHARACTERISTICS

Min. Width of T		50 ns
Max. Rise Time of T		150 ns
Min. Set-Time for D(n) Inputs	1)	100 ns
Delay from T to Q(n) or		
-,Q(n) td1		Min. 10 ns; Typ. 27 ns; Max. 50 ns
td0		Min. 10 ns; Typ. 18 ns; Max. 50 ns
Delay from D(n) to Q(n) or		
-,Q(n) td1 = td0		Typ. 60 ns; Max. 95 ns
Min. Period Time for T		70 + (N-1)x45[ns], N is the number of BD401's.

NOTE

1) To ensure correct storage of data, the C input must be 1 for a time $\geq$ Set-Time, and during this time inputs D(0:2) should remain stable.

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pp. 1:2
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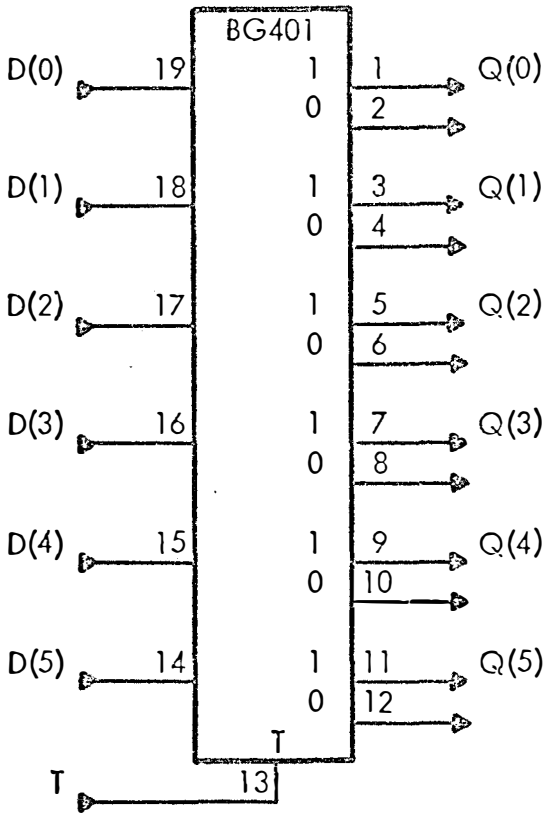
BG401



CIRCUIT DESCRIPTION

The BG401 is a 6-bit parallel-in, parallel-out register element. Data are stored on the transition from 0 to 1 of the clock. The operation is de - scribed in the truth table below.

D(n)	↑ Q(n)
0	0
1	1

↑ Q(n) = Output after the transition from 0 to 1 of the clock.

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

Input Loading

D(n)	1 unit load
T	12 unit loads
Fan-Out	10 unit loads

SWITCHING CHARACTERISTICS

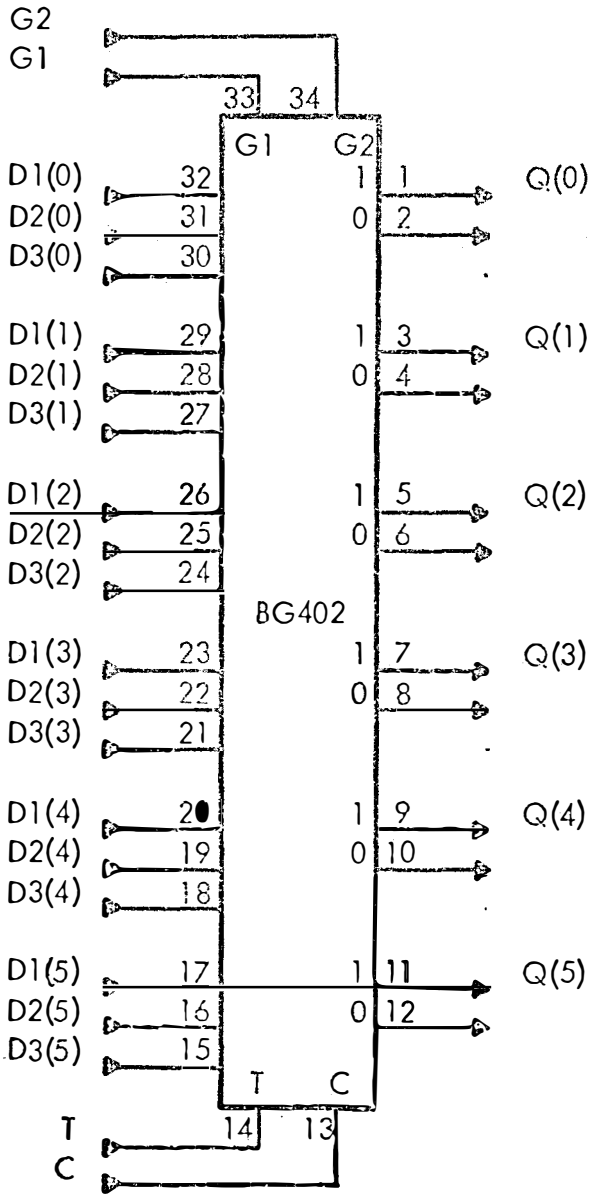
Min. Width of Clock Pulse		30 ns
Max. Clock Frequency		15 Mc/s
Min. Input Set-Up Time	1)	20 ns
Min. Input Hold Time	2)	5 ns
Delay from Clock to Output Q(n) or -,Q(n);	td1	Min. 10 ns, Typ. 20 ns, Max. 35 ns
	td0	Min. 10 ns, Typ. 28 ns, Max. 50 ns

NOTES

1) Set-up time is the time for which the D inputs must be steady before the transition from 0 to 1 of the clock.

2) Hold time is the time for which the D inputs must be steady after the transition from 0 to 1 of the clock.

BG402



CIRCUIT DESCRIPTION

The BG402 is a 6-bit parallel-in, parallel-out register element which is equipped with 2 inputs D1 and D2 for synchronous data entry and 1 input D3 for asynchronous data entry.

Synchronous Data Entry:

Data inputs D1(0:5) and D2(0:5) are controlled by control inputs G1, G2, and the clock input T. Data are stored on the transition from 0 to 1 of the clock.

$X(n) = G1 \wedge D1(n) \vee G2 \wedge D2(n)$

X(n)	↑ Q(n)
0	0
1	1

↑ Q(n) = Output after the transition from 0 to 1 of the clock.

Control input C must be 0 during this mode of operation.

Asynchronous Data Entry:

Data inputs D3(0:5) are controlled by the control input C. Asynchronous data entry is independent of the state of the clock input T.

C	D3(n)	↑ Q(n)
0	0	Q(n)
0	1	Q(n)
1	0	0
1	1	1

Q(n) = Output before the transition from 0 to 1 of C.

↑ Q(n) = Output after the transition from 1 to 0 of C.

When control input C = 1, the output Q(n) will follow the data input D3(n), Qn = D3(n). The logic value of D3(n) is stored when C changes from 1 to 0.

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

Input Loading	
D inputs	1 unit load
G1, G2	6 unit loads
C, T	12 unit loads
Fan-Out	10 unit loads

SWITCHING CHARACTERISTICS

Synchronous Data Entry:			
Min. Width of Clock Pulse			30 ns
Max. Clock Frequency			15 Mc/s
Min. Input Set-Up Time		1)	
G1, G2, D1(0:5), D2(0:5)			50 ns
Min. Input Hold Time		2)	
G1, G2, D1(0:5), D2(0:5)			1 ns
Delay from T to Output			
Q(n) or -,Q(n),	td1		Min. 10 ns; Typ. 20 ns; Max. 35 ns
	td0		Min. 10 ns; Typ. 28 ns; Max. 50 ns
Asynchronous Data Entry:			
Min. Set-Time		3)	75 ns
Delay from D3(n) to Q(n)			
or -,Q(n):	td1		Max. 70 ns
	td0		Max. 85 ns

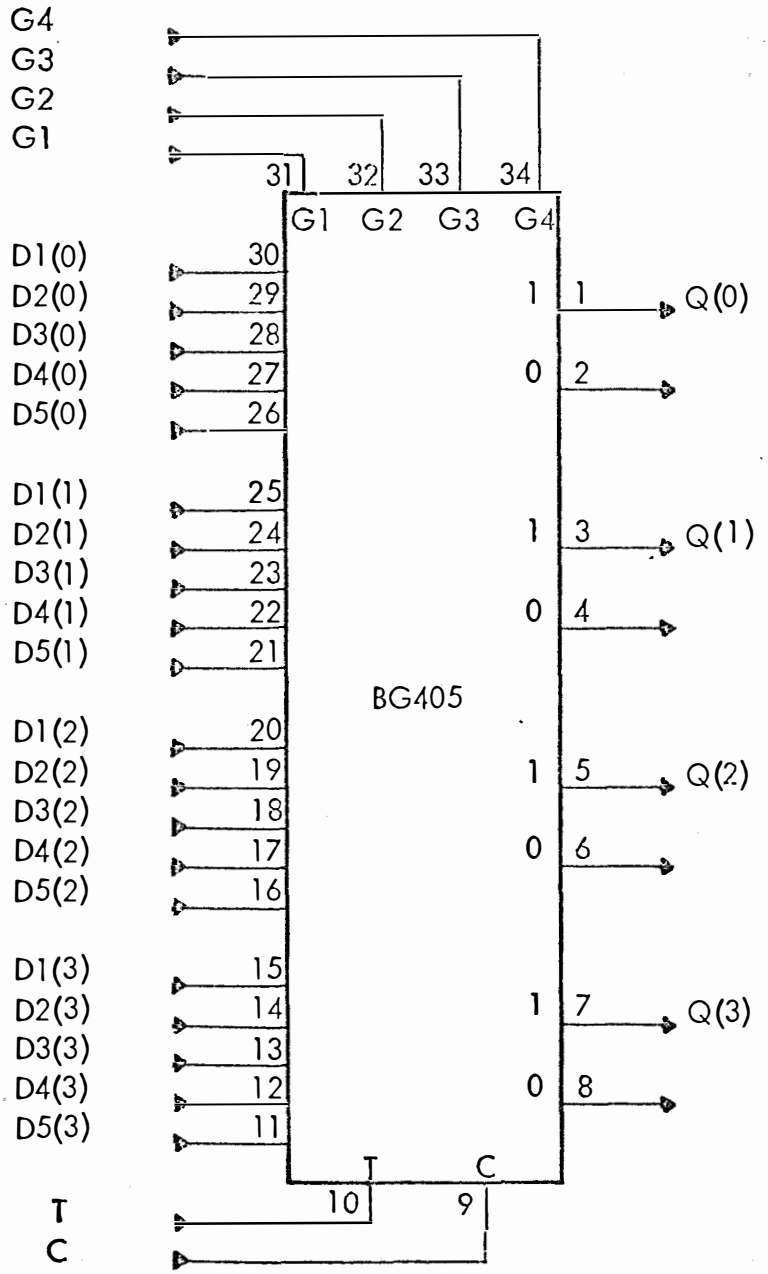
NOTES

1) Set-up time is the time for which the inputs must be steady before the transition from 0 to 1 of the clock.

2) Hold time is the time for which the inputs must be steady after the transition from 0 to 1 of the clock.

3) Set-time is the time for which the C input must be 1 to ensure correct storage of data. During this time the data inputs D3(0:5) should remain stable.

BG405



CIRCUIT DESCRIPTION

The BG405 is a 4-bit parallel-in, parallel-out register element which is equipped with 4 inputs D1, D2, D3, and D4 for synchronous data entry and 1 input D5 for asynchronous data entry.

Synchronous Data Entry:
Data inputs D1(0:3), D2(0:3), D3(0:3), and D4(0:3), are controlled by control inputs G1, G2, G3, G4, and the clock input T. Data are stored on the transition from 0 to 1 of the clock.

$X(n) = G1 \wedge D1(n) \vee G2 \wedge D2(n) \vee G3 \wedge D3(n) \vee G4 \wedge D4(n)$

X(n)	↑ Q(n)
0	0
1	1

↑ Q(n) = Output after the transition from 0 to 1 of the clock.

Control input C must be 0 during this mode of operation.

Asynchronous Data Entry:
Data inputs D5(0:3) are controlled by the control input C. Asynchronous data entry is independent of the state of the clock input T.

C	D5(n)	↓ Q(n)
0	0	Q(n)
0	1	Q(n)
1	0	0
1	1	1

Q(n) = Output before the transition from 0 to 1 of C.

↓ Q(n) = Output after the transition from 1 to 0 of C.

When control input C = 1, the output Q(n) will follow the data input D5(n), Qn = D5(n). The logic value of D5(n) is stored when C changes from 1 to 0.

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

Input Loading	
D inputs	1 unit load
G1, G2, G3, G4	4 unit loads
C, T	8 unit loads
Fan-Out	10 unit loads

SWITCHING CHARACTERISTICS

Synchronous Data Entry:

Min. Width of Clock Pulse		30 ns
Max. Clock Frequency		15 Mc/s
Min. Input Set-Up Time G1, G2, G3, G4, D1(0:3), D2(0:3), D3(0:3), D4(0:3)	1)	50 ns
Min. Input Hold Time G1, G2, G3, G4, D1(0:3), D2(0:3), D3(0:3), D4(0:3)	2)	1 ns
Delay from T to Output Q(n) or -,Q(n),	td1	Min. 10 ns; Typ. 20 ns; Max. 35 ns
	td0	Min. 10 ns; Typ. 28 ns; Max. 50 ns

Asynchronous Data Entry:

Min. Set-Time	3)	75 ns
Delay from D5(n) to Q(n) or -,Q(n),	td1	Max. 70 ns
	td0	Max. 85 ns

NOTES

1) Set-up time is the time for which the inputs must be steady before the transition from 0 to 1 of the clock.

2) Hold time is the time for which the inputs must be steady after the transition from 0 to 1 of the clock.

3) Set-time is the time for which the C input must be 1 to ensure correct storage of data. During this time the data inputs D5(0:3) should remain stable.

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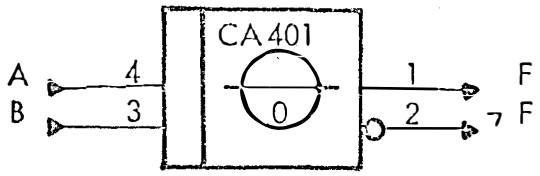
June 1969

CA401

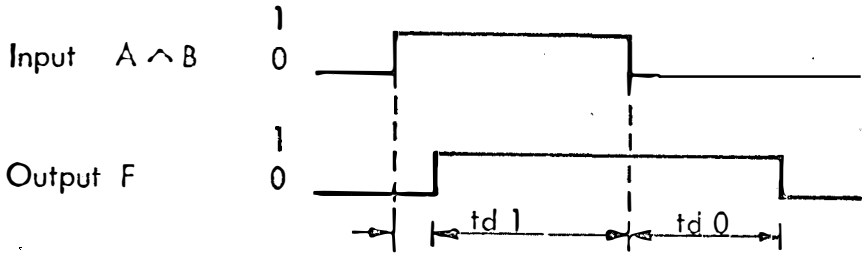


CIRCUIT DESCRIPTION

The CA401 is a delay circuit with adjustable delay of 0.

Coarse adjustment of the delay is obtained by replacement of the timing capacitor C (refer to the PCBA diagram). A continuous adjustment of approximately ±33 per cent is possible by means of a potentiometer.

The figure below shows the operation of the circuit.



SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

Input Loading	1 unit load (each input)
Fan-Out: F	8 unit loads
-.F	10 unit loads

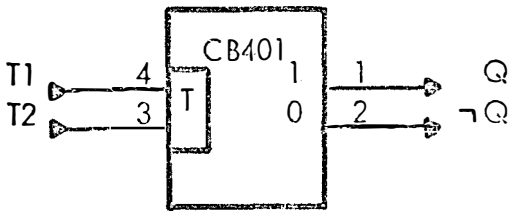
SWITCHING CHARACTERISTICS

Delay from Input to Output F		
Potentiometer max. CCW:	td1	Typ. 16 ns
	td0	Typ. 45 + 0.35x5.1xC [pF,ns]
Potentiometer max. CW:	td1	Typ. 16 ns
	td0	Typ. 60 + 0.35x10.1xC [pF,ns]
Delay from Input to Output -,F		
Potentiometer max. CCW:	td1	Typ. 65 + 0.35x5.1xC [pF,ns]
	td0	Typ. 25 ns
Potentiometer max. CW:	td1	Typ. 75 + 0.35x10.1xC [pF,ns]
	td0	Typ. 25 ns
Variation of td0 for ±5 per cent		
Power Supply Variation		< ±1.5 per cent
Variation of td0 vs.		
Temperature Variation 1)		< +0.05 per cent/deg. C

NOTE

1) Variation of the timing capacitor C is not included.

CB401



CIRCUIT DESCRIPTION

The CB401 is a monostable multivibrator with trigger inputs. The output pulse width is independent of the input pulse width.

The CB401 is triggered when the input function $F = T1 \wedge T2$ changes from 0 to 1.

The output pulse width is continuous variable in a ratio 1.5:1 by means of a screwdriver adjustment. Coarse adjustment is obtained by replacement of the timing capacitor C (refer to the PCBA circuit diagram).

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

Input Loading	1 unit load
Fan-Out: Q	9 unit loads
-,Q	10 unit loads

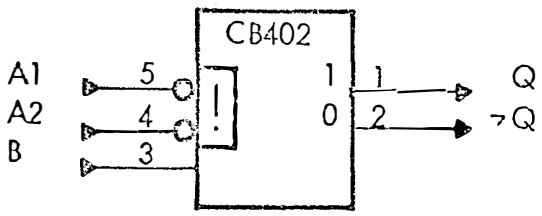
SWITCHING CHARACTERISTICS

Min. Input Pulse Width	100 ns
Output Pulse Width	Tmin = 5×(C+20); [ns,pF] Tmax = 7.5×(C+20); [ns,pF]
Min. Output Pulse Width for C = 0	200 ns
Min. Recovery Time	Tr = Tmin = 5(C+20); [ns,pF]
Variation of Output Pulse Width vs. Power Supply (±5 per cent)	< ±3 per cent
Variation of Output Pulse Width vs. Temperature (0:70° C), 1)	< ±1.5 per cent
Delay from T1, T2 to Q, td1	Typ. 50 ns; Max. 85 ns
Delay from T1, T2 to -,Q, td0	Typ. 60 ns; Max. 100 ns

NOTE

1) Variation of the timing capacitor C is not included.

CB402



CIRCUIT DESCRIPTION

The CB402 is a monostable multivibrator with triggering on positive or negative going inputs. The output pulse width is independent of the input pulse width.

The CB402 is triggered when the input function F = (-,A1 ∨ -,A2) ∧ B changes from 0 to 1. Input B is a schmitt-trigger input which allows triggering on input signals with transition times up to 1 volt/second.

The output pulse width is continuous variable in a ratio 6:1 by means of a screwdriver adjustment. Coarse adjustment is obtained by replacement of the timing capacitor C (refer to the PCBA circuit diagram).

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

Input Loading: A1, A2	1 unit load
B	2 unit loads
Fan-Out	10 unit loads

SWITCHING CHARACTERISTICS

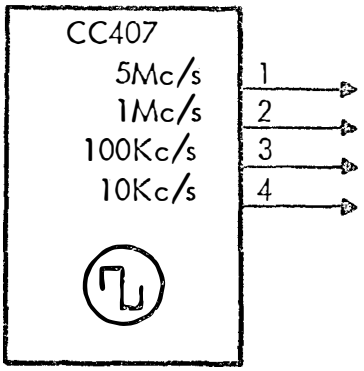
Min. Input Pulse Width		50 ns
Max. Input Rise and Fall Time:		
A1, A2		1 volt/us
B		1 volt/s
Threshold Levels for Input B		
at 25 deg. C: Upper		Typ. 1.55 volt
Lower		Typ. 1.35 volt
Typ. Output Pulse Width		0.69xRxC [ns, kohm, pF] Rmin. = 2 kohms Rmax. = 12 kohms
Min. Output Pulse Width		50 ns; C = 0, R = 2 kohms
Min. Recovery Time 1)		2.8xC [ns,pF]
Delay from A1, A2 to Q:	td1	Min. 25 ns; Typ. 45 ns; Max. 70 ns
Delay from B to Q:	td1	Min. 15 ns; Typ. 35 ns; Max. 55 ns
Delay from A1, A2 to -,Q:	td0	Min. 30 ns; Typ. 50 ns; Max. 80 ns
Delay from B to -,Q:	td0	Min. 20 ns; Typ. 40 ns; Max. 65 ns
Variation of Pulse Width for ±5 per cent Power Supply Variation		Typ. ±0.2 per cent
Variation of Pulse Width with Temperature (0:70 deg. C) 2)		Typ. ±0.2 per cent

NOTES

1) Shorter recovery time is possible if a certain amount of output pulse width reduction is allowed. Some approximate values for output pulse with reduction, delta T versus recovery time Tr, is given below.
   Delta T = 1 per cent for Tr = 2.5 xC [ns,pF]
   Delta T = 5 per cent for Tr = 1.3 xC [ns,pF]
   Delta T = 10 per cent for Tr = 0.71xC [ns,pF]

2) Variation of the timing capacitor C is not included.

CC407

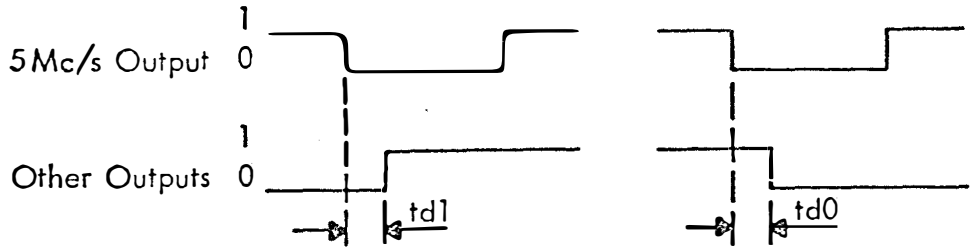


CIRCUIT DESCRIPTION

The CC407 is a precision frequency source with output frequencies of 5 Mc/s, 1 Mc/s, 100 Kc/s, and 10 Kc/s. It comprises a 5 Mc/s crystal controlled oscillator mounted in a proportional-controlled oven, and a ripple counter for frequency division.

The oscillator frequency may be trimmed by means of a screwdriver adjustment.

The delay between the 5 Mc/s output and the 1 Mc/s, 100 Kc/s, and 10 Kc/s outputs are measured as shown below.



It should be noted that the card occupies the same space as 7 normal cards.

SPECIFICATIONS:

ELECTRICAL CHARACTERISTICS

Fan-Out	
5 Mc/s output	6 unit loads
1 Mc/s, 100 Kc/s, and 10 Kc/s outputs	10 unit loads (each output)

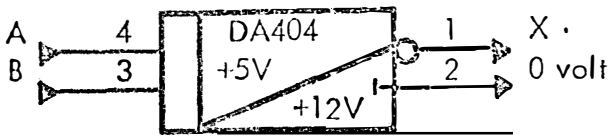
SWITCHING CHARACTERISTICS

Stability vs. Temperature	Typ. $\pm 5 \times 10^{-9}$/deg. C
Stability vs. Supply Voltage	Typ. $\pm 2.5 \times 10^{-8}$ for a ±5 per cent variation of +12V supply
Average Aging Rate	$+2 \times 10^{-8}$/day
Warm-up Accuracy	Better than 1×10^{-6} after 1 minute. Better than 1×10^{-7} after 3 minutes.
Output Duty Cycle, 5 Mc/s	Approximately 50 per cent
1 Mc/s	20 per cent
100 Kc/s	50 per cent
10 Kc/s	50 per cent
Delay between 5 Mc/s output and	
1 Mc/s output: td1	Typ. 20 ns; Max. 35 ns
td0	Typ. 20 ns; Max. 35 ns
100 Kc/s output: td1	Typ. 60 ns; Max. 105 ns
td0	Typ. 60 ns; Max. 105 ns
10 Kc/s output: td1	Typ. 100 ns; Max. 175 ns
td0	Typ. 100 ns; Max. 175 ns

MECHANICAL

The card occupies the same space as 7 normal cards.

DA404



CIRCUIT DESCRIPTION

The DA404 is a digital level converter for coupling RCLM400 modules to systems requiring higher voltage swing. The DA404 accepts RCLM400 standard signal levels at inputs A and B. The nominal output voltage levels at X are 0 volt and +12 volts. The 0-volt terminal may e.g. be used for twisted pairs.

The logical operation of the circuit is $X = \neg(A \wedge B) = \neg A \vee \neg B$.

SPECIFICATIONS

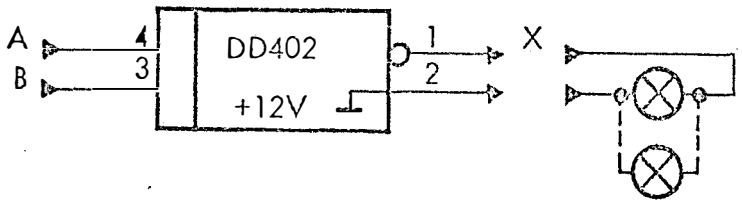
ELECTRICAL CHARACTERISTICS

Input Levels	RCLM400 standard signal levels
Input Loading: A,B	1 unit load
Output High:	
Output Voltage	Vout = 12-volt supply (output unloaded)
Output Impedance	440 ohms ±10 per cent
Output Low:	
Output Voltage	$0\ V \leq Vout \leq 0.5\ V$
Output Current	$-23\ mA \leq Iout \leq +50\ mA$ 1)

NOTE

1) The sign is positive when the current flows towards the circuit.

DD402



CIRCUIT DESCRIPTION

The DD402 is a lamp driver for incandescent lamps, type CM330, 14 V, 80 mA or equivalent.

The logical operation of the circuit is: $X = \neg(A \wedge B)$. I.e. the lamp will be lit when A and B are 1.

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

Input Loading	1 unit load
Output Drive Capability	Max. two CM330, 14 V, 80 mA or equivalent connected in parallel.
Max. Output Load Current	150 mA

SWITCHING CHARACTERISTICS

Min. Duration of On-Time	1)	10 us
Min. Duration of Off-Time		40 us

NOTE

1) On-time is the time the output is 0.

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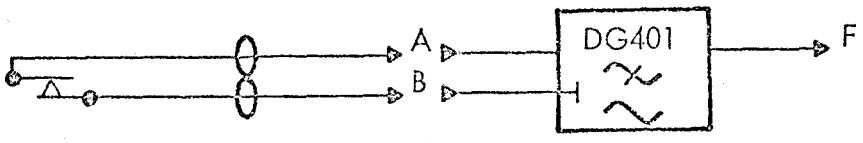
July 1969

DG401



CIRCUIT DESCRIPTION

The DG401 is a low-pass filter intended to be used as an interface element between mechanical switches and RCLM400 modules. The switch is connected to the DG401 with a twisted pair as shown above.

Output F is 0 when the switch is closed (A and B shorted) and 1 when the switch is open.

The maximum cable length between the switch and the DG401 is determined by the maximum resistance between A and B which will ensure a 0 at the output of the DG401.

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

Max. Input Current in A when shorted to B	-(2.9 + N×1.6)mA N is the fan-out. 1)
Voltage at A with open Input	Min. +3.5 V; Max. +4.3 V The voltage is measured relative to B.
Max. Resistance between A and B for a 0	64 ohms for fan-out = 1 27 ohms for fan-out = 2 9 ohms for fan-out = 3

Min. Resistance between A and B for a 1	4.1 kohms for fan-out = 1 4.4 kohms for fan-out = 2 4.7 kohms for fan-out = 3

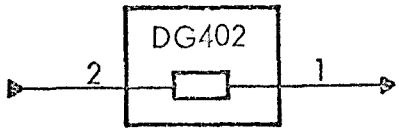
SWITCHING CHARACTERISTICS

Time Constant for pos. Slope	Approximately 36 µs
Time Constant for neg. Slope	Approximately 1.5 µs

NOTE

1) The sign is positive when the current flows towards the circuit.

DG402



CIRCUIT DESCRIPTION

The DG402 is an interface element which is used to connect the output of a logic element to the DM160 indicator tube.

The connection of the DG402 and the DM160 indicator tube is shown on page 2. The tube will be lit when a logical 1 is applied to the DG402. No light indicates a 0. The length of the wire between the DG402 and the DM160 is not critical.

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

Input Loading	negligible

SWITCHING CHARACTERISTICS

Output Drive Capability	1 DM160 indicator tube

INTERCONNECTION OF DG402 and DM160